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(54) Advanced electrolytic polish assisted metal wafer planarization

(57) In advanced electrolytic polish (AEP) method, a metal wafer (10) acts as an anodic electrodes and another metal plate (65) is used as a cathodic electrode. A voltage differential is applied to the anode and cathode under a predetermined anodic dissolution current density. This causes a reaction that provides a planarized surface on the metal wafers. Additives are included in the electrolyte solution (55) which adsorb onto the wafer surface urging a higher removal rate at higher spots and a lower removal rate at lower spots. Also, in another embodiment of the present invention is a pulsed-electrolytic process (260) in which positive and negative potentials are applied to the anodic and cathodic electrodes alternately, further encouraging surface planarization. AEP can be used either as a first step followed by a mechanical polish or a second step between initial CMP polish and a third step mechanical polish. The present invention may also be added as a last step of copper electroplating process and so may be used in the manufacture of all kinds of patterned metal wafers.

FIG. 2.

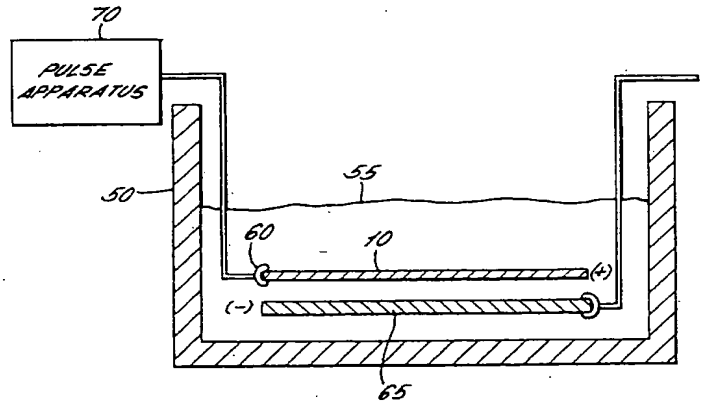

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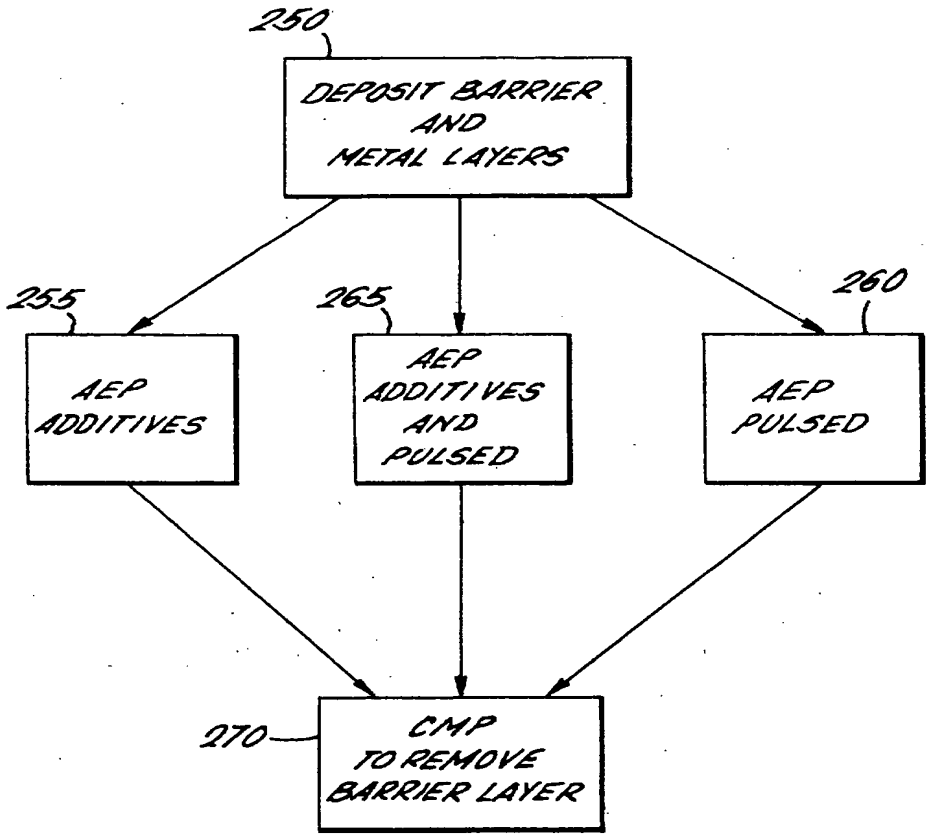
FIG. 5.


250
DEPOSIT BARRIER AND METAL LAYERS
255
AEP ADDITIVES
265
AEP ADDITIVES AND PULSED
260
AEP PULSED
270
CMP TO REMOVE BARRIER LAYER

Description

[0001] This invention relates generally to planarization of metal substrates and more particularly to advanced electrolytic polishing of metal films on semiconductor wafers.

[0002] Integrated circuits are typically formed on substrates, particularly silicon wafers, by the sequential deposition of conductive,, semiconductive or insulative layers. After a layer is deposited, the layer is etched to create circuitry features. As a series of layers are sequentially deposited and etched, the outer or uppermost surface of the substrate, i.e., the exposed surface of the substrate, becomes increasingly non-planar. This non-planar outer surface presents a problem for the integrated circuit manufacturer. Therefore, there is a need to periodically planarize the substrate surface to provide a relatively flat surface. In some fabrication processes, planarization of the outer layer should not expose underlying layers.

[0003] Chemical mechanical polishing (CMP) is a current method of planarization. This planarization method typically requires that the substrate be mounted on a carrier or polishing head. The exposed surface of the substrate is placed against a rotating polishing pad. The polishing pad may be either a "standard" pad or a fixed-abrasive pad. A fixed-abrasive pad has abrasive particles held in a containment media, whereas a standard pad has a durable surface, without embedded abrasive particles. The carrier head provides a controllable load, i.e., pressure, on the substrate to push it against the polishing pad. A polishing slurry, including at least one chemically-reactive agent, and abrasive particles if a standard pad is used, is supplied to the surface of the polishing pad.

[0004] An effective CMP process not only provides a high polishing rate, but also provides a substrate surface which is finished and flat. The polishing rate, finish and flatness are determined by the pad and slurry combination, the relative speed between the substrate and pad, and the force pressing the substrate against the pad.

[0005] In applying conventional planarization techniques, such as CMP, it is extremely difficult to achieve a high degree of surface uniformity, particularly across a surface extending from a dense array of features, for example copper lines, bordered by an open field. A dense array of metal features is typically formed in an interlayer dielectric, such as silicon oxide layer, by a damascene technique wherein trenches are initially formed. A barrier layer, such as a Ta-containing layer e. g. Ta, TaN, is then deposited lining the trenches and on the upper surface of the silicon oxide interlayer dielectric. Copper or a copper alloy is then deposited, as by electroplating, electroless plating, physical vapor deposition (PVD) at a temperature of about 50°C to about 150°C or chemical vapor deposition (CVD) at a temperature under about 200°C, typically at a thickness of about 8000Å to about 18,000Å. In planarizing the wafer surface after copper metallization using CMP, undesirable erosion and dishing typically occur, decreasing the degree of surface uniformity or planarity and challenging the depth of focus limitations of conventional photolithographic techniques, particular with i respect to achieving submicron dimensions, such as about 0.25 micron. Erosion is defined as the height differential between the oxide in the open field and the height of the oxide within the dense array. Dishing is defined as a difference in height between the oxide and Cu within the dense array.

[0006] Dishing and erosion formation are the most important parameters in evaluating metal CMP processes. Current processes using CMP generate at best 600-800Å dishing and 400

- 1500Å erosion, depending on the pattern density on the substrate. There are generally two causes for dishing formation: a) insufficient planarization and b) over-polish. CMP accomplishes planarization, but the efficiency of the planarization decreases significantly as the feature size increases on the substrate. Over-polish is performed to remove metal residue from a wafer's surface after CMP. Over-polish contributes significantly to dishing and erosion formation, especially when over-polish is done at a relatively high polish rate in order to have high throughput. Past efforts to improve dishing and erosion included modifications to the slurry, polishing pad and the process.

[0007] It remains desirable to have a process of planarization where dishing and erosion are decreased.

[0008] It is an advantage of the present invention to provide a method and apparatus for substrate planarization producing a good quality substrate surface with high throughput.

[0009] The problems of reducing dishing and erosion while achieving planarized processed substrates are solved by the present invention of an advanced electrolytic polish (AEP) assisted metal wafer planarization method and apparatus.

[0010] The advanced electrolytic polish (AEP) method polishes the metal surface of a layered substrate in a controlled way so that higher spots are removed more quickly than lower spots in the surface topography. AEP uses a reverse electroplating method along with surface modifying methods, either alone or in combination, to remove material from a substrate in order to planarize the substrate. A first surface modifying method is to include surface modifying additives in the electrolyte solution used for AEP. A second surface modifying method is pulsed electrolysis with application of alternating positive and negative potentials, in which the potential across the electrodes in AEP is periodically reversed causing high points on the substrate surface to be removed before low points on the substrate surface. Additives and pulsed electrolysis can be combined in an AEP process.

[0011] The polish in the present embodiment of the invention stops when a barrier layer (e.g.tantalum, tantalum nitride, titanium or titanium nitride) is substantially removed. Alteration of the electrolyte chemistry of the present invention, however, would alter the depth and the layers removed in the polish. Additives to the electrolyte solution, and the application of pulsed voltage during electrolytic polish further improve the planarity of the substrate polished surface.

[0012] In the AEP method herein described, substrates act as anodic electrodes and another metal plate is used as a cathodic electrode. The substrate and the cathode are configured in either an electroplating tank or in an adapted chemical mechanical polishing device. A voltage differential is applied to the anode and cathode under a predetermined anodic dissolution current density. This causes a reaction that provides a planarized surface on the metal wafers. Current electrolytic polishing methods generally leave at least 500A difference between high and low spots in the wafer surface topography. With the present advanced electrolytic polish, additives are included in the electrolyte solution which adsorb onto the wafer surface urging a higher removal rate at higher spots and a lower removal rate at lower spots. Also, another embodiment of the present invention is a pulsed-electrolytic process in which positive and negative potentials are applied to the anodic and cathodic electrodes alternately, further encouraging surface planarization. A further embodiment of the invention involves using the additive method and the pulsed method in combination.

[0013] AEP can be used either as a first step followed by a short mechanical polishing step (buffing) to remove the thin barrier layer (250Å); or as a second step between an initial CMP polish with about 2000Å copper layer remaining and a third step mechanical polish. The present invention may also be added as a last step of copper electroplating process and so may be used in the manufacture of all kinds of patterned metal wafers.

[0014] With the AEP technique, the "insufficient planarization" problem that occurs in normal CMP processes is substantially eliminated, the first CMP step is much easier, and dishing and erosion caused by the over-polishing step are avoided. AEP eliminates erosion because there is no mechanical action during the AEP process. This is particularly important in processing wafers having high density surface patterns where there is a high potential for erosion. Dishing is greatly decreased with the chemical additives and the pulsed current. The AEP method provides a planarized surface without erosion and with very little dishing.

[0015] The present invention together with the above and other advantages may best be understood from the following detailed description of the embodiments of the invention illustrated in the drawings.

Figure 1 is a cross-sectional view of a substrate with a plurality of layers;

Figure 2 is a cross-sectional view of a first embodiment of an advanced electrolytic polish device wherein a wafer is immersed in a tank having an electrolyte solution according to principles of the present invention;

Figure 3 is a simplified cross--sectional view of a second embodiment of an advanced electrolytic polish device wherein a polishing head contains anodes and a cathode according to principles of the present invention;

Figure 4 is a schematic exploded view of a chemical mechanical polishing apparatus;

Figure 5 is a flow chart of a first embodiment of a polishing step using AEP according to principles of the present invention; and,

Figure 6 is a flow chart of a second embodiment of a polishing step using AEP according to principles of the present invention.

[0016] Figure 1 shows a cross-sectional view of a conductive substrate 10 having deposited layers such as those layers formed during the manufacture of semiconductors. The figure is not to scale. An interlayer dielectric 20, e.g. silicon oxide, is formed overlying a metal wafer 15. A plurality of indentations, also referred to as openings 25, are formed in a designated area at the left of the interlayer dielectric 20 in which a dense array of conductive lines are to be formed bordering an open field shown on the right of the interlayer dielectric 20. A barrier layer 30, e.g. tantalum, tantalum nitride, titanium or titanium nitride, is deposited on the layer of interlayer dielectric 20, the barrier layer 30 also lining the plurality of openings 25. A conductive layer 35, e.g. copper, is then deposited over the barrier layer 30. The successive layers forms an uneven topography 36 over the substrate which requires planarization before further processing. Also, successive process steps require that portions of the conductive layer be removed. Planarization and selective removal of the conductive layer are accomplished in a polishing step.

[0017] Figure 2 shows a side cross-sectional view of an electrolyzer in a first embodiment of the present invention of advanced electrolytic polishing (AEP). The conductive substrate 10 of Figure 1 is immersed in a tank 50 containing a solution 55 of electrolytes. The conductive substrate 10 is connected to a conductive clamp 60 to form a first electrode, an anode. A second electrode 65, a cathode matching the metal substrate is also immersed in the tank 50. A voltage differential is applied to the anode and cathode under a predetermined anodic dissolution current density. The current density is typically 1 - 30 mA/cm^2. This causes a reaction that provides a planarized surface on conductive substrates. The reaction when the barrier layer is substantially exposed,

leaving a planarized surface on the substrate having conductive areas and substantially exposed barrier layer. Current electrolytic polishing methods generally leave at least 500Å difference between high and low spots in the wafer surface topography.

[0018] Additives are included in the electrolyte solution which adsorb onto the substrate surface urging a higher removal rate at higher spots and a lower removal rate at lower spots. The additives are generally less than 1% of the electrolyte solution by weight. The additives are surface modifiers. The adsorbed additives act as electric discharge points that modify the surface of the substrate so that high spots are polished first and then low spots are polished. Examples of additives used in this process are coumarin ($C_9H_6O_2$), sulfourea ($CS(NH_2)_2$), and $R\text{-}C_6H_5\text{-}O\text{-}(CH_3CH_2O)_n$, where R= C_8-C_9, and n=10. Other additives and concentrations are possible within the scope of the present invention.

[0019] Also, in an alternative embodiment of the present invention, a pulsed-electrolytic process is applied, using a pulse apparatus 70, in which positive and negative potentials are applied between the anodic and cathodic electrodes alternately, further encouraging surface planarization. The pulse apparatus may be an alternator, or a potentiostat with pulsing capability. In this method, a current density typically in the range of 1 - 30 mA/cm^2, for example, is applied typically for a few milliseconds. The pulse-polish modifies the surface of the substrate. Material from high spots on the surface is redeposited to low spots on the surface. This is a useful surface modification in those cases where planarization is not sufficient.

[0020] Figure 3 shows a simplified, part cross-sectional, part schematic, side view of an even further embodiment of the present invention of AEP. In Figure 3, a polish head 100 rests on a polish pad 105 with the metal substrate 10 of Figure 1 in between the head 100 and the pad 105. An anodic connection 110 and a cathodic connection 115 are provided. The anodic connection contacts the substrate 10 such that the substrate becomes an anode. In the present embodiment of the invention, the anodic 110 and cathodic 115 connections form rings around the head inside the retaining ring 120. A membrane 118 between the polish head and the substrate 10 provides pressure to maintain the contact between the anodic connection 110 and the substrate 10 and between the substrate 10 and polish pad 105. First 116 and second 117 brushes provide electrical connection from connections 110, 115 to an electrolysis controller 119. The electrolysis controller 119 may include a pulse apparatus 70 such as that shown in Figure 2. A metal portion of the retaining ring 120 acts as a cathode 122. The placement of anodes 110, 115 and the cathode 122 are merely exemplary. Other configurations are possible within the scope of the present invention.

[0021] The pad 105 is wetted with electrolyte solution 121. A slurry arm 225 (shown in Figure 4) having tubes for slurry, in this case for electrolyte solution, extends over the polishing pad 105. A voltage differential is applied to the anode substrate 10 and the cathode 122. This causes a reaction that provides a planarized surface on the conductive substrate. The head 100 spins in order to carry polishing product away from the wafer 10, however, mechanical polishing does not take place. Additives are added to the electrolyte solution with the same effect as described above. No abrasion of the wafer is necessary in order to accomplish the polishing. The pulse polish technique may also be used in this configuration.

[0022] Figure 4 shows a chemical mechanical polishing apparatus 200 having a plurality of polishing stations 205, 210, 215. One of the polish heads on the apparatus 200 has modifications as shown in Figure 3 in order to accomplish the present invention. The head 220 of polishing station 205 has an anodic connection 110, and a cathode 122 as seen in Figure 3. Slurry arm 225 delivers electrolyte solution to the polishing pad 105. Alternatively, one or more of the polishing stations could be modified with the electrochemical cell shown in Figure 2 in order to accomplish the present invention.

[0023] Figure 5 is a flow chart of a first embodiment of a polishing step using AEP according to principles of the present invention. After the barrier layer and the metal layer have been deposited on the wafer, block 250, AEP is applied to planarize the wafer. The planarization may be accomplished by AEP using additives, block 255, AEP using pulsed current, block 260, or AEP using both additives and pulsed current, block 265. Then CMP is applied to the wafer to remove the barrier layer, block 270.

[0024] Figure 6 is a flow chart of a second embodiment of a polishing step using AEP according to principles of the present invention. After the barrier layer and the metal layers have been deposited on the wafer, block 300, CMP is applied, block 305, until a thin film of metal of a predetermined thickness remains, for example 2000Å. Then AEP is applied to remove the remaining metal and to planarize the surface of the wafer. The AEP process may be AEP using i additives, block 310, AEP using pulsed current, block 315, or AEP using both additives and pulsed current, block 320. CMP is then applied to the wafer to remove the barrier layer, block 325.

[0025] It is to be understood that the above-described embodiments are simply illustrative of the principles of the invention. Various and other modifications and changes may be made by those skilled in the art which will embody the principles of the invention and fall within the spirit and scope thereof.

Claims

1. A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:

advanced electrolytic polishing (AEP) the substrate until the barrier layer is substantially exposed forming a planarized surface; and
chemical mechanical polishing the substrate until the barrier layer is substantially removed from the planarized surface of the substrate leaving a smooth surface containing selected amounts of conductive material.

2. A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:

providing a cathodic electrode;
providing an anodic electrode for electrical connection to the substrate;
providing an electrolyte solution, said anodic electrode and cathodic electrode in contact with said electrolyte solution;
applying a voltage differential between said anodic electrode and said cathodic electrode;
modifying the surface of said substrate in order to remove material from high spots on the surface before removing material from low spots, whereby said wafer is planarized by electrolytically removing material from the surface as effected by modifying the surface of the substrate, the removal process stopping at the barrier layer.

3. A method as claimed in claim 2, wherein said surface modifying step further comprises the step of including additives in said electrolyte solution to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface.

4. A method as claimed in claim 3, wherein said additive is coumarin.

5. A method as claimed in claim 3, wherein said additive is sulfourea.

6. A method as claimed in claim 3, wherein said additive is C_8-C_6-H_5-$O(CH_3CH_2O)_{10}$.

7. A method as claimed in claim 3, wherein said additive is C_9-C_6-H_5-$O(CH_3CH_2O)_{10}$.

8. A method as claimed in any of claims 2 to 7, wherein said surface modifying step further comprises the step of applying positive and negative potentials alternately between electrodes.

9. A method as claimed in claim 8, wherein said positive and negative potentials are applied over periods of milliseconds.

10. A method as claimed in claim 8 or claim 9, wherein said surface modifying step further comprises the steps of using an electrolyte solution containing an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface; and applying positive and negative potentials alternately between electrodes.

11. A method as claimed in any of claims 2 to 10, further comprising the steps of providing a tank holding a quantity of said electrolyte solution; and submerging said anodic electrode and said cathodic electrode in said electrolyte solution, wherein said substrate is an anode.

12. A method as claimed in any of claims 2 to 11, further comprising the steps of adapting a polish head to carry electrodes to connect with the substrate to form an anode and a retaining ring to form a cathode; and wetting a polishing pad with electrolyte solution.

13. A method of polishing a substrate, said substrate having a barrier layer below a metal layer, comprising the steps of:

chemical mechanical polishing the substrate until a predetermined thickness of the metal layer is reached;
advanced electrolytic polishing (AEP) of the substrate until the barrier layer is exposed and the substrate is substantially planarized; and
chemical mechanical polishing the substrate until the barrier layer is substantially removed from the planarized surface of the substrate.

14. A method as claimed in claim 13, wherein said AEP step further comprises the step of using an electrolyte solution containing an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface.

15. A method as claimed in claim 14, wherein said additive is coumarin.

16. A method as claimed in claim 14, wherein said additive is sulfourea.

17. A method as claimed in any of claims 13 to 16, wherein said AEP step further comprises the step of applying positive and negative potentials alternately between electrodes.

18. A method as claimed in claim 17, wherein said positive and negative potentials are applied over periods of milliseconds.

19. A method as claimed in claim 17 or claim 18, wherein said AEP step further comprises the steps of using an electrolyte solution containing an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface; and

applying positive and negative potentials alternately between electrodes.

20. A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:

providing an anodic connection to the substrate making the substrate an anode;
providing a cathode;
providing an electrolyte solution in contact with both said anode and said cathode, said electrolyte solution containing an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface;
providing current to said anode to remove material from said anode until the barrier layer is exposed thereby forming a planarized surface on the substrate; and
further polishing the substrate until the barrier layer is substantially removed from the planarized surface of the substrate leaving a smooth surface containing selected amounts of conductive surface.

21. A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:

providing an anodic connection to the substrate making the substrate an anode;
providing a cathode;
providing an electrolyte solution in contact with both said anode and said cathode;
applying positive and negative potentials alternately between said anode and said cathode to remove material from said anode until the barrier layer is exposed thereby forming a planarized surface on the substrate; and
further polishing the substrate until the barrier layer is substantially removed from the planarized surface of the substrate leaving a smooth surface containing selected amounts of conductive surface.

22. A method as claimed in claim 21, wherein said electrolyte solution contains an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface.

23. A method of forming a planarized layer on a substrate, comprising the steps of:

forming an interlayer dielectric having an upper surface and a plurality of openings;
depositing a barrier layer on said upper surface of said interlayer dielectric, said barrier layer also lining said plurality of openings;
depositing a conductive layer on said barrier layer, said conductive layer filling said lined plurality of openings,
advanced electrolytic polishing (AEP) the substrate until said barrier layer is substantially exposed forming a planarized surface; and
further polishing the substrate until said barrier layer is substantially removed from said planarized surface of the substrate having a planarized layer containing selected amounts of conductive material.

24. A chemical mechanical polishing (CMP) apparatus adapted for advanced electrolytic polishing (AEP) of a substrate, comprising:

an anode located in a polishing head of said CMP apparatus, said anode contacting the substrate held in said polishing head;
a cathode located in said polishing head, said cathode offset from said anode;
a polishing pad wetted with an electrolyte solution, said electrolyte solution and the substrate providing a connection between said anode and said cathode; and
an electrolysis controller to provide a potential across said anode and said cathode, said electrolysis controller alternating said potential between positive and negative,
whereby said substrate is planarized without mechanical action of the CMP apparatus.

25. An apparatus as claimed in claim 24, wherein said electrolyte solution further comprises an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface.

26. An apparatus as claimed in claim 24 or claim 25, wherein said electrolysis controller further comprises a pulse apparatus for alternating said potential.

27. An apparatus as claimed in any of claims 24 to 26, wherein said anode further comprises a ring around said polishing head forming an anodic connection from said electrolysis controller to said substrate.

28. An apparatus as claimed in any of claims 24 to 27, wherein said cathode is a portion of a retaining ring in said polishing head.

29. A chemical mechanical polishing (CMP) apparatus adapted for advanced electrolytic polishing (AEP) of a substrate, comprising:

an anode located in a polishing head of said CMP apparatus, said anode contacting a substrate held in said polishing head;
a cathode located in said polishing head, said cathode offset from said anode; and
a polishing pad wetted with an electrolyte solution, said electrolyte solution having an additive to urge higher removal rates at higher spots on the substrate surface and lower removal rates at lower spots on the substrate surface, said electrolyte solution providing an electrical connection between said anode and said cathode;
an electrolysis controller to provide a potential across said anode and said cathode;
whereby said substrate is planarized without mechanical action of the CMP apparatus.

30. An apparatus as claimed in claim 29, wherein said additive is coumarin.

31. An apparatus as claimed in claim 29, wherein said additive is sulfourea.

32. An apparatus as claimed in claim 29, wherein said additive is C_8-C_6H_5-O-$(CH_3CH_2O)_{10}$.

33. An apparatus as claimed in claim 29, wherein said additive is C_9-C_6C_5-O-$(CH_3CH_2O)_{10}$.

FIG. 1.

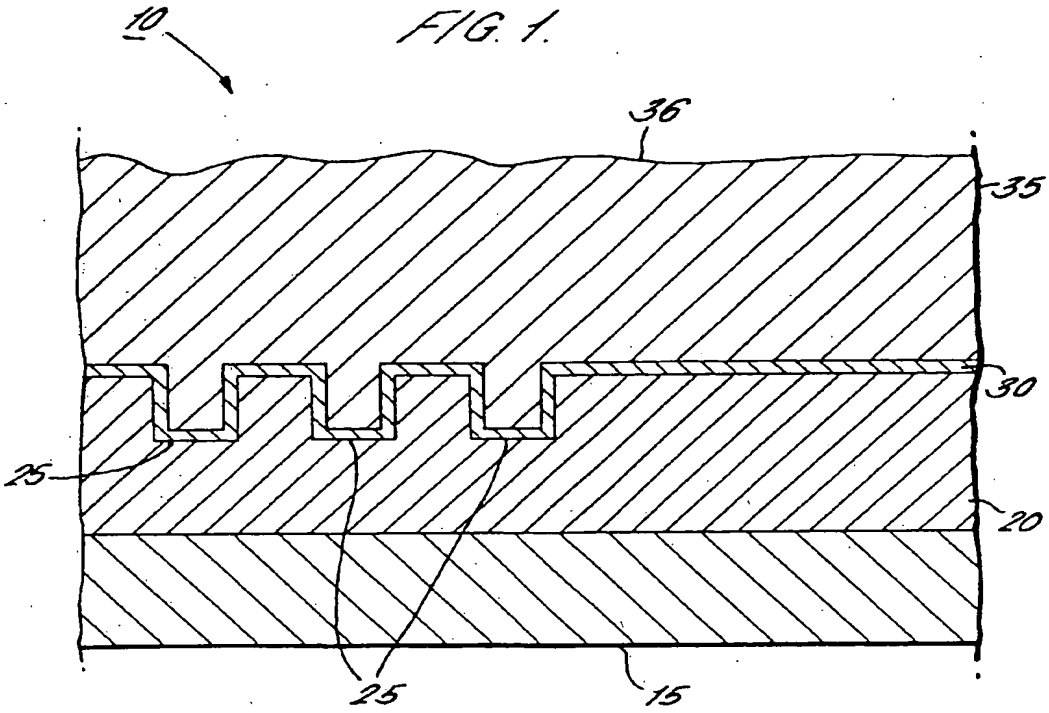


FIG. 2.

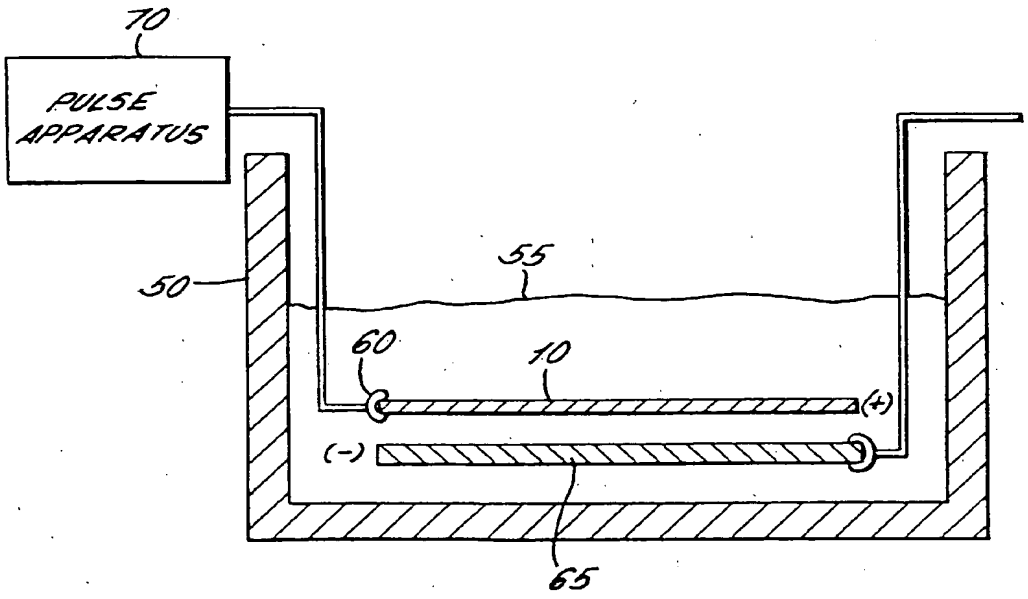
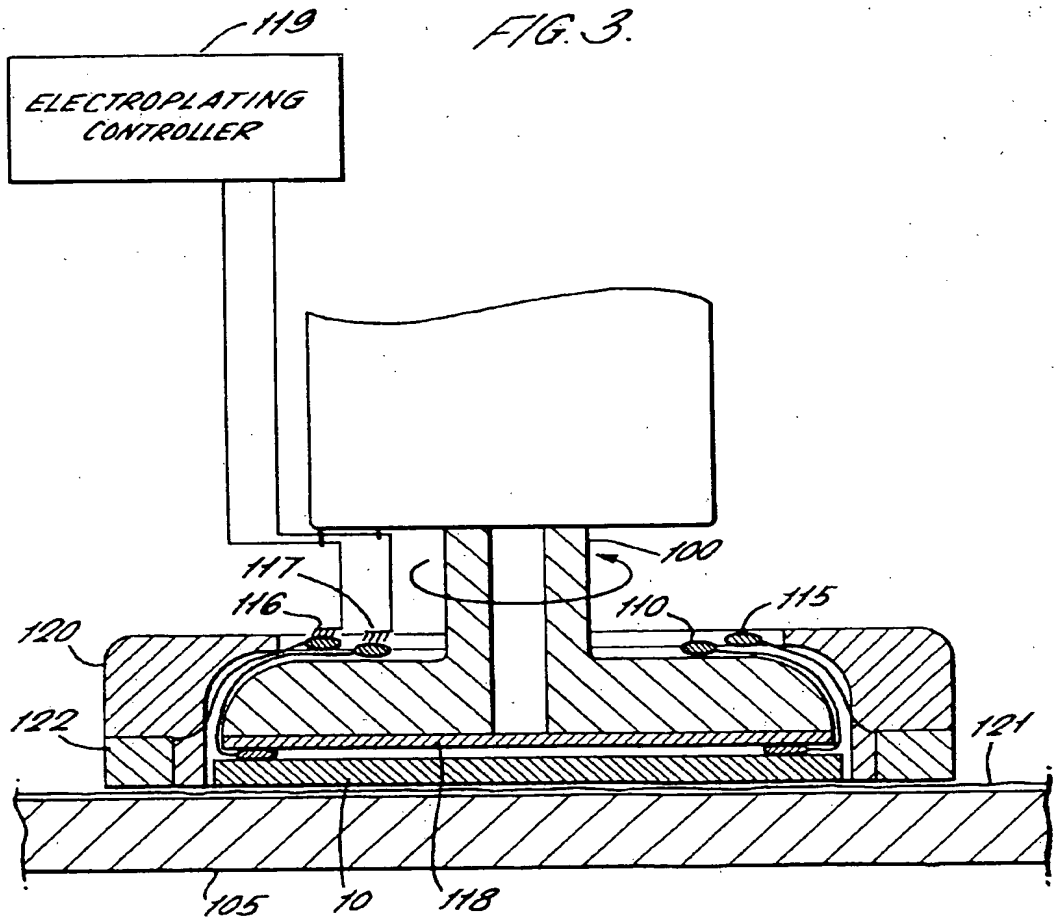


FIG. 3.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ELECTROPLATING CONTROLLER
100
117
116
110
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118

FIG. 4.

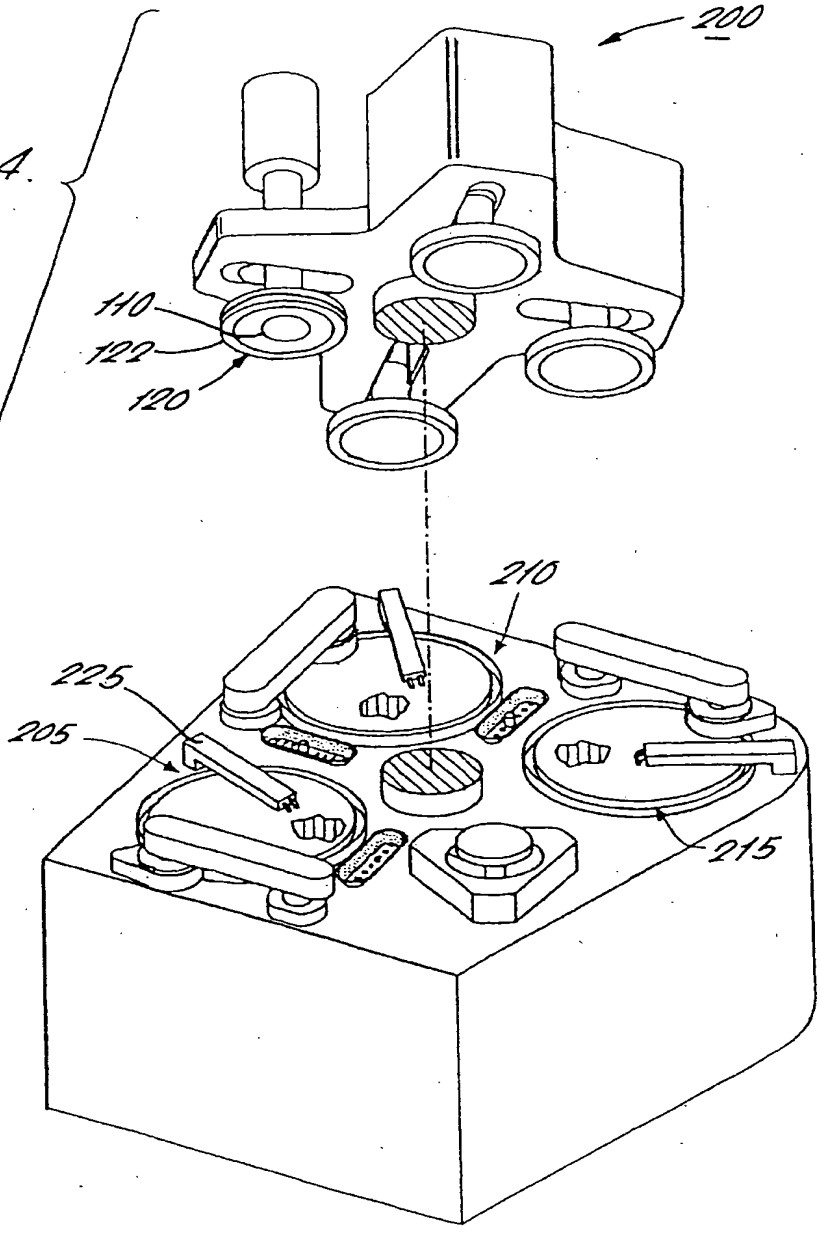
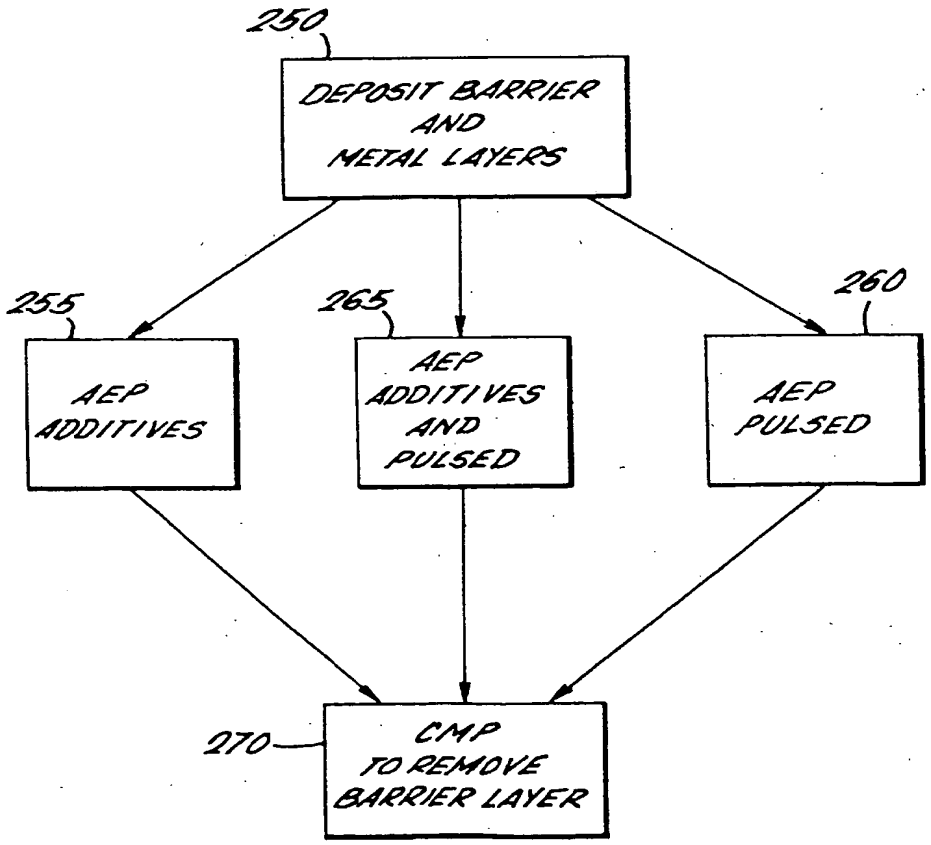


FIG. 5.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DEPOSIT BARRIER AND METAL LAYERS
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AEP ADDITIVES
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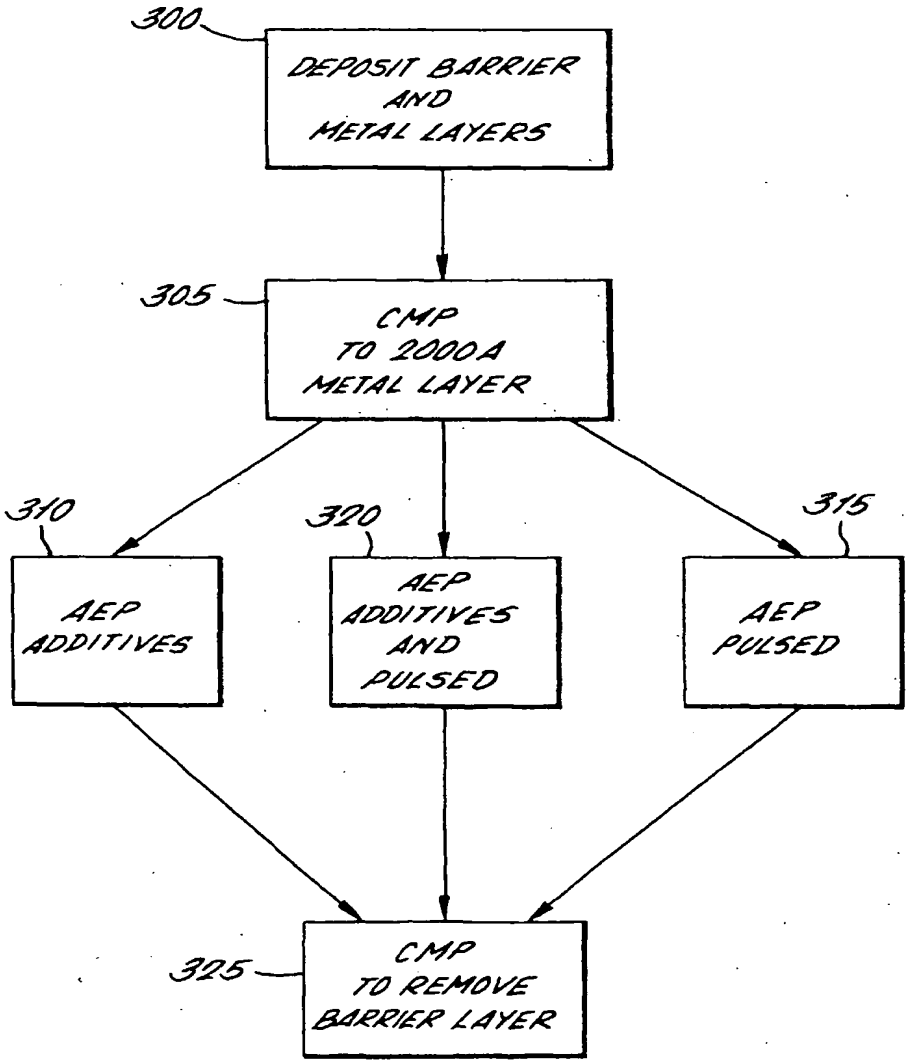
AEP ADDITIVES AND PULSED
260
AEP PULSED
270
CMP TO REMOVE BARRIER LAYER

FIG. 6.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AEP ADDITIVES
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AEP ADDITIVES AND PULSED
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325
CMP TO REMOVE BARRIER LAYER

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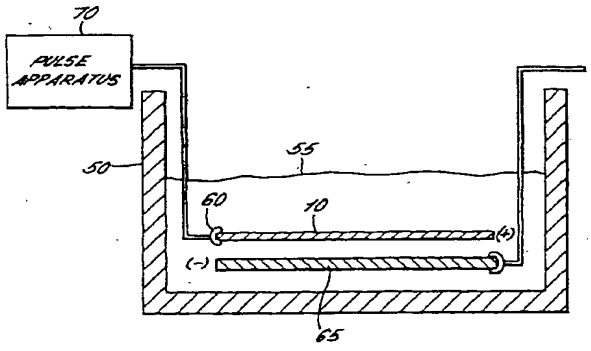
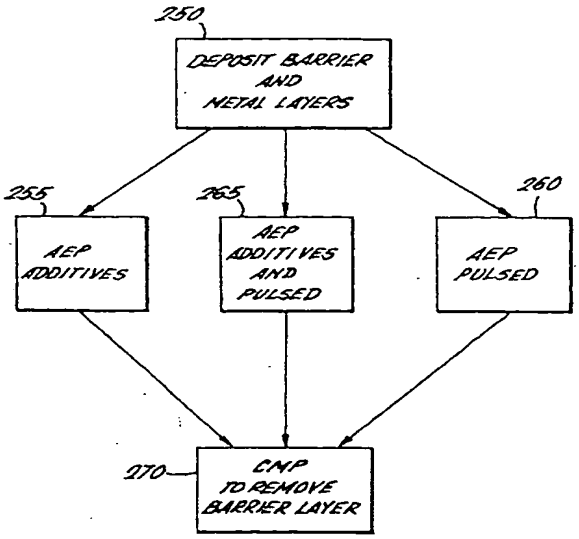
(57) In advanced electrolytic polish (AEP) method, a metal wafer (10) acts as an anodic electrodes and another metal plate (65) is used as a cathodic electrode. A voltage differential is applied to the anode and cathode under a predetermined anodic dissolution current density. This causes a reaction that provides a planarized surface on the metal wafers. Additives are included in the electrolyte solution (55) which adsorb onto the wafer surface urging a higher removal rate at higher spots and a lower removal rate at lower spots. Also, in another embodiment of the present invention is a pulsed-electrolytic process (260) in which positive and negative potentials are applied to the anodic and cathodic electrodes alternately, further encouraging surface planarization. AEP can be used either as a first step followed by a mechanical polish or a second step between initial CMP polish and a third step mechanical polish. The present invention may also be added as a last step of copper electroplating process and so may be used in the manufacture of all kinds of patterned metal wafers.

FIG. 2.



EP 1 104 013 A3

FIG. 5.


250
DEPOSIT BARRIER AND METAL LAYERS
255
AEP ADDITIVES
265
AEP ADDITIVES AND PULSED
260
AEP PULSED
270
CMP TO REMOVE BARRIER LAYER

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 31 0560

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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X	CONTOLINI R J ET AL: "ELECTROCHEMICAL PLANARIZATION OF ULSI COPPER" SOLID STATE TECHNOLOGY, COWAN PUBL.CORP. WASHINGTON, US, vol. 40, no. 6, 1 June 1997 (1997-06-01), pages 155-156,158,160, XP000656403 ISSN: 0038-111X * page 155; figure 1 * * page 156, right-hand column *	1,13	
X	US 5 807 165 A (HARPER JAMES MCKELL EDWIN ET AL) 15 September 1998 (1998-09-15) * column 4, line 55 - column 5, line 41 *	1,13,17, 18	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
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A	US 5 567 300 A (DATTA MADHAV ET AL) 22 October 1996 (1996-10-22) * the whole document *		

-/--

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
The Hague	21 November 2003	Szarowski, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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Application Number
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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 13, 30 November 1999 (1999-11-30) -& JP 11 238703 A (NEC CORP), 31 August 1999 (1999-08-31) * abstract * -----		

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
The Hague	21 November 2003	Szarowski, A

CATEGORY OF CITED DOCUMENTS

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Application Number
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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1, 13-19

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LACK OF UNITY OF INVENTION
SHEET B

Application Number
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The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1,13-19

A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:
- electrolytic polishing the substrate until the barrier layer is exposed forming a planarized surface; and
- chemical mechanical polishing the substrate until the barrier layer is removed from the planarized surface of the substrate.

---

2. claim: 20

A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:
- electrolytic polishing the substrate until the barrier layer is exposed forming a planarized surface, wherein the electrolyte contains an additive; and

- further polishing the substrate until the barrier layer is removed from the planarized surface of the substrate.

---

3. claims: 21,22

A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:
- electrolytic polishing the substrate until the barrier layer is exposed forming a planarized surface, wherein positive and negative potentials are alternately applied to the electrodes; and
- further polishing the substrate until the barrier layer is removed from the planarized surface of the substrate.

---

4. claim: 23

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

A method of forming a planarized layer on a substrate, comprising the steps of:
- forming an interlayer dielectric having an upper surface and a plurality of openings;
- depositing a barrier layer lining said openings;

- depositing a conductive layer on said barrier layer;

- electrolytic polishing the substrate until said barrier layer is exposed forming a planarized surface; and
- further polishing the substrate until said barrier layer is removed from said planarized surface of the substrate.

---

5. claims: 2-12,24-33

A method of polishing a substrate, said substrate including a barrier layer below a conductive layer, comprising the steps of:
- modifying the surface of said substrate in order to remove material from high spots on the surface before removing material from low spots, wherein said wafer is planarized by electrolytically removing material from the surface as effected by modifying the surface of the substrate, the removal process stopping at the barrier layer.

Apparatus therefor.

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO. EP 00 31 0560

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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